IN THE CLAIMS

Please cancel claims 9-14.

Please amend the claims as follows.

1. (Original) An apparatus comprising:

at least one processor;

a memory coupled to the at least one processor;

an integrated circuit design residing in the memory, the integrated circuit design including a plurality of logic blocks;

a static timing tool residing in the memory and executed by the at least one processor, the static timing tool performing analysis that results in a plurality of slack computations;

a timing analysis mechanism residing in the memory and executed by the at least one processor, the timing analysis mechanism including a dummy edge mechanism that creates a dummy clock test edge for a selected logic block that has a clock test signal and a data launch signal that are on opposite edges in a manner that results in the dummy clock test edge and the data launch signal being on the same edge, the static timing tool automatically identifying in the integrated circuit design at least one common logic block through which the clock test signal and the data launch signal both pass before arriving at the selected logic block, the timing analysis mechanism automatically improving at least one of the plurality of slack computations due to the at least one common logic block.

2. (Original) The apparatus of claim 1 wherein the static timing tool is EinsTimer.

3. (Original) The apparatus of claim 1 wherein the timing analysis mechanism determines a difference between fastest and slowest delay through the at least one common logic block, multiplies the difference by a correction factor, and adjusts the slack by the difference multiplied by the correction factor.

4. (Original) The apparatus of claim 1 wherein the timing analysis mechanism improves at least one of the plurality of slack computations using at least one user delta adjust parameter to adjust the clock test signal.

5. (Original) The apparatus of claim 1 wherein the timing analysis mechanism provides input to the static timing tool but is not part of the static timing tool.

6. (Original) An apparatus comprising:

at least one processor;

a memory coupled to the at least one processor;

an integrated circuit design residing in the memory, the integrated circuit design including a plurality of logic blocks;

a static timing tool residing in the memory and executed by the at least one processor, the static timing tool performing analysis that results in a plurality of slack computations; and

a timing analysis mechanism residing in the memory and executed by the at least one processor, the timing analysis mechanism being separate from the static timing tool and providing input to the static timing tool, wherein the timing analysis mechanism creates a dummy clock test edge for a selected logic block that has a clock test signal and a data launch signal that are on opposite edges in a manner that results in the dummy clock test edge and the data launch signal being on the same edge, the static timing tool automatically identifying in the integrated circuit design at least one common logic block through which the clock test signal and the data launch signal both pass before arriving at the selected logic block, the timing analysis mechanism automatically improving at least one of the plurality of slack computations due to the at least one common logic block using at least one user delta adjust parameter to adjust the clock test signal.

7. (Original) The apparatus of claim 6 wherein the static timing tool is EinsTimer.

8. (Original) The apparatus of claim 6 wherein the timing analysis mechanism determines a difference between fastest and slowest delay through the at least one common logic block, multiplies the difference by a correction factor, and adjusts the slack by the difference multiplied by the correction factor.

9-14 (Cancelled)

15. (Original) A program product comprising:

a timing analysis mechanism that includes a dummy edge mechanism that creates a dummy clock test edge for a selected logic block in an integrated circuit design, the selected logic block having a clock test signal and a data launch signal that are on opposite edges, the dummy edge mechanism creating the dummy clock test edge so the dummy clock test edge and the data launch signal are on the same edge, the timing analysis mechanism automatically identifying in the integrated circuit design at least one common logic block through which the clock test signal and the data launch signal both pass before arriving at the selected logic block, the timing analysis mechanism automatically improving at least one of the plurality of slack computations due to the at least one common logic block; and

computer readable signal bearing media bearing the timing analysis mechanism.

16. (Original) The program product of claim 15 wherein the signal bearing media comprises recordable media.

17. (Original) The program product of claim 15 wherein the signal bearing media comprises transmission media.

18. (Original) The program product of claim 15 wherein the static timing tool is EinsTimer.

19. (Original) The program product of claim 15 wherein the timing analysis mechanism determines a difference between fastest and slowest delay through the at least one common logic block, multiplies the difference by a correction factor, and adjusts the slack by the difference multiplied by the correction factor.

20. (Original) The program product of claim 15 wherein the timing analysis mechanism improves at least one of the plurality of slack computations using at least one user delta adjust parameter to adjust the clock test signal.

21. (Original) A program product comprising:

a timing analysis mechanism that is separate from a static timing tool and that provides input to the static timing tool, the timing analysis mechanism creating a dummy clock test edge for a selected logic block that has a clock test signal and a data launch signal that are on opposite edges in a manner that results in the dummy clock test edge and a data launch signal on a logic block in an integrated circuit design occurring on the same edge, the timing analysis mechanism automatically identifying in the integrated circuit design at least one common logic block through which the clock test signal and the data launch signal both pass before arriving at the selected logic block, the timing analysis mechanism automatically improving at least one of the plurality of slack computations due to the at least one common logic block using at least one user delta adjust parameter to adjust the clock test signal; and

computer readable signal bearing media bearing the timing analysis mechanism.

22. (Original) The program product of claim 21 wherein the signal bearing media comprises recordable media.

23. (Original) The program product of claim 21 wherein the signal bearing media comprises transmission media.

24. (Original) The program product of claim 21 wherein the static timing tool is EinsTimer.

25. (Original) The program product of claim 21 wherein the timing analysis mechanism determines a difference between fastest and slowest delay through the at least one common logic block, multiplies the difference by a correction factor, and adjusts the slack by the difference multiplied by the correction factor.

STATUS OF THE CLAIMS

Claims 1-25 were originally filed in this patent application. In the pending office action, claims 1-25 were subject to restriction. In this amendment, claims 9-14 have been cancelled. Claims 1-8 and 15-25 are currently pending.